1 **HAVING BIOMATERIAL COMPONENT OR INTEGRATED WITH LIVING ORGANISM**
2 **HAVING SUPERCONDUCTIVE COMPONENT**
3 **HAVING MAGNETIC OR FERROELECTRIC COMPONENT**
4 **REPAIR OR RESTORATION**
5 **INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION**
6 .Interconnecting plural devices on semiconductor substrate
7 .Optical characteristic sensed
8 ..Chemical etching
9 ...Plasma etching
10 .Electrical characteristic sensed
11 ..Utilizing integral test element
12 ..And removal of defect
13 ..Altering electrical property by material removal
14 **WITH MEASURING OR TESTING**
15 .Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
16 .Optical characteristic sensed
17 .Electrical characteristic sensed
18 ..Utilizing integral test element
19 **HAVING INTEGRAL POWER SOURCE (E.G., BATTERY, ETC.)**
20 **ELECTRON EMITTER MANUFACTURE**
21 **MANUFACTURE OF ELECTRICAL DEVICE CONTROLLED PRINTHEAD**
22 **MAKING DEVICE OR CIRCUIT EMISSIVE OF NONELECTRICAL SIGNAL**
23 .Having diverse electrical device
24 ..Including device responsive to nonelectrical signal
25 ...Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
26 .Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
27 ..Having additional optical element (e.g., optical fiber, etc.)
28 ..Plural emissive devices
29 .Including integrally formed optical element (e.g., reflective layer, luminescent material, contoured surface, etc.)
30 ..Liquid crystal component
31 ..Optical waveguide structure
32 ..Optical grating structure
33 .Substrate dicing
34 .Making emissive array
35 ..Multiple wavelength emissive
36 .Ordered or disordered
37 .Graded composition
38 .Passivating of surface
39 .Mesa formation
40 ..Tapered etching
41 ..With epitaxial deposition of semiconductor adjacent mesa
42 .Groove formation
43 ..Tapered etching
44 ..With epitaxial deposition of semiconductor in groove
45 .Dopant introduction into semiconductor region
46 .Compound semiconductor
47 ..Heterojunction
48 **MAKING DEVICE OR CIRCUIT RESPONSIVE TO NONELECTRICAL SIGNAL**
49 .Chemically responsive
50 .Physical stress responsive
51 ..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
52 ..Having cantilever element
53 ..Having diaphragm element
54 .Thermally responsive
55 ..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
56 .Responsive to corpuscular radiation (e.g., nuclear particle detector, etc.)
57 .Responsive to electromagnetic radiation
58 ..Gettering of substrate
59 ..Having diverse electrical device
60 ...Charge transfer device (e.g., CCD, etc.)
61 ..Continuous processing
62 ...Using running length substrate
63 ..Particulate semiconductor component

64 ..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
65 ...Having additional optical element (e.g., optical fiber, etc.)
66 ...Plural responsive devices (e.g., array, etc.)
67 ....Assembly of plural semiconductor substrates
68 ..Substrate dicing
69 ..Including integrally formed optical element (e.g., reflective layer, luminescent layer, etc.)
70 ...Color filter
71 ...Specific surface topography (e.g., textured surface, etc.)
72 ...Having reflective or antireflective component
73 ..Making electromagnetic responsive array
74 ...Vertically arranged (e.g., tandem, stacked, etc.)
75 ...Charge transfer device (e.g., CCD, etc.)
76 ....Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)
77 ....Compound semiconductor
78 ....Having structure to improve output signal (e.g., exposure control structure, etc.)
79 .....Having blooming suppression structure (e.g., antiblooming drain, etc.)
80 ...Lateral series connected array
81 ....Specified shape junction barrier (e.g., V-grooved junction, etc.)
82 ..Having organic semiconductor component
83 ..Forming point contact
84 ..Having selenium or tellurium elemental semiconductor component
85 ..Having metal oxide or copper sulfide compound semiconductive component
86 ...And cadmium sulfide compound semiconductive component
87 ..Graded composition
88 ..Direct application of electric current
89 ..Fusion or solidification of semiconductor region
90 ..Including storage of electrical charge in substrate
91 ..Avalanche diode
92 ..Schottky barrier junction
93 ..Compound semiconductor
94 ...Heterojunction
95 ...Chalcogen (i.e., oxygen (O), sulfur (S), selenium (Se), tellurium (Te)) containing
96 ..Amorphous semiconductor
97 ..Polycrystalline semiconductor
98 ..Contact formation (i.e., metallization)
99 **HAVING ORGANIC SEMICONDUCTIVE COMPONENT**
100 **MAKING POINT CONTACT DEVICE**
101 .Direct application of electrical current
102 **HAVING SELENIUM OR TELLURIUM ELEMENTAL SEMICONDUCTOR COMPONENT**
103 .Direct application of electrical current
104 **HAVING METAL OXIDE OR COPPER SULFIDE COMPOUND SEMICONDUCTOR COMPONENT**
105 **HAVING DIAMOND SEMICONDUCTOR COMPONENT**
106 **PACKAGING (E.G., WITH MOUNTING, ENCAPSULATING, ETC.) OR TREATMENT OF PACKAGED SEMICONDUCTOR**
107 .Assembly of plural semiconductive substrates each possessing electrical device
108 ..Flip-chip-type assembly
109 ..Stacked array (e.g., rectifier, etc.)
110 .Making plural separate devices
111 ..Using strip lead frame
112 ...And encapsulating
113 ..Substrate dicing
114 ...Utilizing a coating to perfect the dicing
115 .Including contaminant removal or mitigation
116 .Having light transmissive window
117 .Incorporating resilient component (e.g., spring, etc.)
118 .Including adhesive bonding step

119 ..Electrically conductive adhesive
120 .With vibration step
121 .Metallic housing or support
122 ..Possessing thermal dissipation structure (i.e., heat sink)
123 ..Lead frame
124 ..And encapsulating
125 .Insulative housing or support
126 ..And encapsulating
127 .Encapsulating
128 **MAKING DEVICE ARRAY AND SELECTIVELY INTERCONNECTING**
129 .With electrical circuit layout
130 .Rendering selected devices operable or inoperable
131 .Using structure alterable to conductive state (i.e., antifuse)
132 .Using structure alterable to nonconductive state (i.e., fuse)
133 **MAKING REGENERATIVE-TYPE SWITCHING DEVICE (E.G., SCR, IGBT, THYRISTOR, ETC.)**
134 .Bidirectional rectifier with control electrode (e.g., triac, diac, etc.)
135 .Having field effect structure
136 ..Junction gate
137 ...Vertical channel
138 ..Vertical channel
139 .Altering electrical characteristic
140 .Having structure increasing breakdown voltage (e.g., guard ring, field plate, etc.)
141 **MAKING CONDUCTIVITY MODULATION DEVICE (E.G., UNIJUNCTION TRANSISTOR, DOUBLE BASE DIODE, CONDUCTIVITY-MODULATED TRANSISTOR, ETC.)**
142 **MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS**
143 .Gettering of semiconductor substrate
144 .Charge transfer device (e.g., CCD, etc.)
145 ..Having additional electrical device
146 ..Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)
147 ..Changing width or direction of channel (e.g., meandering channel, etc.)
148 ..Substantially incomplete signal charge transfer (e.g., bucket brigade, etc.)
149 .On insulating substrate or layer (e.g., TFT, etc.)
150 ..Specified crystallographic orientation
151 ..Having insulated gate
152 ...Combined with electrical device not on insulating substrate or layer
153 ....Complementary field effect transistors
154 ...Complementary field effect transistors
155 ...And additional electrical device on insulating substrate or layer
156 ...Vertical channel
157 ...Plural gate electrodes (e.g., dual gate, etc.)
158 ...Inverted transistor structure
159 ....Source-to-gate or drain-to-gate overlap
160 ....Utilizing backside irradiation
161 ...Including source or drain electrode formation prior to semiconductor layer formation (i.e., staggered electrodes)
162 ...Introduction of nondopant into semiconductor layer
163 ...Adjusting channel dimension (e.g., providing lightly doped source or drain region, etc.)
164 ...Semiconductor islands formed upon insulating substrate or layer (e.g., mesa formation, etc.)
165 ....Including differential oxidation
166 ...Including recrystallization step
167 .Having Schottky gate (e.g., MESFET, HEMT, etc.)
168 ..Specified crystallographic orientation
169 ..Complementary Schottky gate field effect transistors

170 ..And bipolar device
171 ..And passive electrical device (e.g., resistor, capacitor, etc.)
172 ..Having heterojunction (e.g., HEMT, MODFET, etc.)
173 ..Vertical channel
174 ..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)
175 ..Buried channel
176 ..Plural gate electrodes (e.g., dual gate, etc.)
177 ..Closed or loop gate
178 ..Elemental semiconductor
179 ..Asymmetric
180 ..Self-aligned
181 ...Doping of semiconductive region
182 ....T-gate
183 ....Dummy gate
184 ....Utilizing gate sidewall structure
185 .....Multiple doping steps
186 .Having junction gate (e.g., JFET, SIT, etc.)
187 ..Specified crystallographic orientation
188 ..Complementary junction gate field effect transistors
189 ..And bipolar transistor
190 ..And passive device (e.g., resistor, capacitor, etc.)
191 ..Having heterojunction
192 ..Vertical channel
193 ...Multiple parallel current paths (e.g., grid gate, etc.)
194 ..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)
195 ..Plural gate electrodes
196 ..Including isolation structure
197 .Having insulated gate (e.g., IGFET, MISFET, MOSFET, etc.)
198 ..Specified crystallographic orientation
199 ..Complementary insulated gate field effect transistors (i.e., CMOS)
200 ...And additional electrical device
201 ....Including insulated gate field effect transistor having gate surrounded by dielectric (i.e., floating gate)
202 ....Including bipolar transistor (i.e., BiCMOS)
203 .....Complementary bipolar transistors
204 .....Lateral bipolar transistor
205 .....Plural bipolar transistors of differing electrical characteristics
206 .....Vertical channel insulated gate field effect transistor
207 .....Including isolation structure
208 ......Isolation by PN junction only
209 ....Including additional vertical channel insulated gate field effect transistor
210 ....Including passive device (e.g., resistor, capacitor, etc.)
211 ...Having gate surrounded by dielectric (i.e., floating gate)
212 ...Vertical channel
213 ...Common active region
214 ...Having underpass or crossunder
215 ...Having fuse or integral short
216 ...Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound
217 ...Doping of semiconductor channel region beneath gate insulator (e.g., threshold voltage adjustment, etc.)
218 ...Including isolation structure
219 ....Total dielectric isolation
220 ....Isolation by PN junction only
221 ....Dielectric isolation formed by grooving and refilling with dielectric material
222 .....With epitaxial semiconductor layer formation
223 .....Having well structure of opposite conductivity type
224 ......Plural wells
225 ....Recessed oxide formed by localized oxidation (i.e., LOCOS)
226 .....With epitaxial semiconductor layer formation

227 .....Having well structure of opposite conductivity type
228 ......Plural wells
229 ...Self-aligned
230 ....Utilizing gate sidewall structure
231 .....Plural doping steps
232 ....Plural doping steps
233 ...And contact formation
234 ..Including bipolar transistor (i.e., BiMOS)
235 ...Heterojunction bipolar transistor
236 ...Lateral bipolar transistor
237 ..Including diode
238 ..Including passive device (e.g., resistor, capacitor, etc.)
239 ...Capacitor
240 ....Having high dielectric constant insulator (e.g., Ta2O5, etc.)
241 ....And additional field effect transistor (e.g., sense or access transistor, etc.)
242 .....Including transistor formed on trench sidewalls
243 ....Trench capacitor
244 .....Utilizing stacked capacitor structure (e.g., stacked trench, buried stacked capacitor, etc.)
245 .....With epitaxial layer formed over the trench
246 .....Including doping of trench surfaces
247 ......Multiple doping steps
248 ......Including isolation means formed in trench
249 ......Doping by outdiffusion from a dopant source layer (e.g., doped oxide, etc.)
250 ....Planar capacitor
251 .....Including doping of semiconductive region
252 ......Multiple doping steps
253 ....Stacked capacitor
254 .....Including selectively removing material to undercut and expose storage node layer
255 .....Including texturizing storage node layer
256 .....Contacts formed by selective growth or deposition
257 ..Having additional gate electrode surrounded by dielectric (i.e., floating gate)
258 ...Including additional field effect transistor (e.g., sense or access transistor, etc.)
259 ...Including forming gate electrode in trench or recess in substrate
260 ...Textured surface of gate insulator or gate electrode
261 ...Multiple interelectrode dielectrics or nonsilicon compound gate insulator
262 ...Including elongated source or drain region disposed under thick oxide regions (e.g., buried or diffused bitline, etc.)
263 ....Tunneling insulator
264 ...Tunneling insulator
265 ...Oxidizing sidewall of gate electrode
266 ...Having additional, nonmemory control electrode or channel portion (e.g., for accessing field effect transistor structure, etc.)
267 ....Including forming gate electrode as conductive sidewall spacer to another electrode
268 ..Vertical channel
269 ...Utilizing epitaxial semiconductor layer grown through an opening in an insulating layer
270 ...Gate electrode in trench or recess in semiconductor substrate
271 ....V-gate
272 ....Totally embedded in semiconductive layers
273 ...Having integral short of source and base regions
274 ....Short formed in recess in substrate
275 ..Making plural insulated gate field effect transistors of differing electrical characteristics
276 ...Introducing a dopant into the channel region of selected transistors

277 ....Including forming overlapping gate electrodes
278 ....After formation of source or drain regions and gate electrode (e.g., late programming, encoding, etc.)
279 ..Making plural insulated gate field effect transistors having common active region
280 ..Having underpass or crossunder
281 ..Having fuse or integral short
282 ..Buried channel
283 ..Plural gate electrodes (e.g., dual gate, etc.)
284 ..Closed or loop gate
285 ..Utilizing compound semiconductor
286 ..Asymmetric
287 ..Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound
288 ..Having step of storing electrical charge in gate dielectric
289 ..Doping of semiconductive channel region beneath gate insulator (e.g., adjusting threshold voltage, etc.)
290 ...After formation of source or drain regions and gate electrode
291 ...Using channel conductivity dopant of opposite type as that of source and drain
292 ..Direct application of electrical current
293 ..Fusion or solidification of semiconductor region
294 ..Including isolation structure
295 ...Total dielectric isolation
296 ...Dielectric isolation formed by grooving and refilling with dielectric material
297 ...Recessed oxide formed by localized oxidation (i.e., LOCOS)
298 ....Doping region beneath recessed oxide (e.g., to form chanstop, etc.)
299 ..Self-aligned
300 ...Having elevated source or drain (e.g., epitaxially formed source or drain, etc.)
301 ...Source or drain doping
302 ....Oblique implantation
303 ....Utilizing gate sidewall structure
304 .....Conductive sidewall component
305 .....Plural doping steps
306 ....Plural doping steps
307 .....Using same conductivity-type dopant
308 ..Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)
309 **FORMING BIPOLAR TRANSISTOR BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS**
310 .Gettering of semiconductor substrate
311 .On insulating substrate or layer (i.e., SOI type)
312 .Having heterojunction
313 ..Complementary bipolar transistors
314 ..And additional electrical device
315 ..Forming inverted transistor structure
316 ..Forming lateral transistor structure
317 ..Wide bandgap emitter
318 ..Including isolation structure
319 ...Air isolation (e.g., mesa, etc.)
320 ..Self-aligned
321 ...Utilizing dummy emitter
322 .Complementary bipolar transistors
323 ..Having common active region (i.e., integrated injection logic (I2L), etc.)
324 ...Including additional electrical device
325 ...Having lateral bipolar transistor
326 ..Including additional electrical device
327 ..Having lateral bipolar transistor
328 .Including diode
329 .Including passive device (e.g., resistor, capacitor, etc.)
330 ..Resistor

331 ...Having same doping as emitter or collector
332 ...Lightly doped junction isolated resistor
333 .Having fuse or integral short
334 .Forming inverted transistor structure
335 .Forming lateral transistor structure
336 ..Combined with vertical bipolar transistor
337 ..Active region formed along groove or exposed edge in semiconductor
338 ..Having multiple emitter or collector structure
339 ..Self-aligned
340 .Making plural bipolar transistors of differing electrical characteristics
341 .Using epitaxial lateral overgrowth
342 .Having multiple emitter or collector structure
343 .Mesa or stacked emitter
344 .Washed emitter
345 .Walled emitter
346 .Emitter dip prevention or utilization
347 .Permeable or metal base
348 .Sidewall base contact
349 .Pedestal base
350 .Forming base region of specified dopant concentration profile (e.g., inactive base region more heavily doped than active base region, etc.)
351 .Direct application of electrical current
352 .Fusion or solidification of semiconductor region
353 .Including isolation structure
354 ..Having semi-insulative region
355 ..Total dielectrical isolation
356 ..Isolation by PN junction only
357 ...Including epitaxial semiconductor layer formation
358 ....Up diffusion of dopant from substrate into epitaxial layer
359 ..Dielectric isolation formed by grooving and refilling with dielectrical material
360 ...With epitaxial semiconductor formation in groove
361 ...Including deposition of polysilicon or noninsulative material into groove
362 ..Recessed oxide by localized oxidation (i.e., LOCOS)
363 ...With epitaxial semiconductor layer formation
364 .Self-aligned
365 ..Forming active region from adjacent doped polycrystalline or amorphous semiconductor
366 ...Having sidewall
367 ....Including conductive component
368 ...Simultaneously outdiffusing plural dopants from polysilicon or amorphous semiconductor
369 ..Dopant implantation or diffusion
370 ...Forming buried region (e.g., implanting through insulating layer, etc.)
371 ...Simultaneous introduction of plural dopants
372 ....Plural doping steps
373 .....Multiple ion implantation steps
374 ......Using same conductivity-type dopant
375 .....Forming partially overlapping regions
376 .....Single dopant forming regions of different depth or concentrations
377 .....Through same mask opening
378 .Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)
379 **VOLTAGE VARIABLE CAPACITANCE DEVICE MANUFACTURE (E.G., VARACTOR, ETC.)**
380 **AVALANCHE DIODE MANUFACTURE (E.G., IMPATT, TRAPPAT, ETC.)**
381 **MAKING PASSIVE DEVICE (E.G., RESISTOR, CAPACITOR, ETC.)**
382 .Resistor
383 ..Lightly doped junction isolated resistor
384 ..Deposited thin film resistor
385 ...Altering resistivity of conductor

386 .Trench capacitor
387 ..Having stacked capacitor structure (e.g., stacked trench, buried stacked capacitor, etc.)
388 ..With epitaxial layer formed over the trench
389 ..Including doping of trench surfaces
390 ...Multiple doping steps
391 ...Including isolation means formed in trench
392 ...Doping by outdiffusion from a dopant source layer (e.g., doped oxide)
393 .Planar capacitor
394 ..Including doping of semiconductive region
395 ...Multiple doping steps
396 .Stacked capacitor
397 ..Including selectively removing material to undercut and expose storage node layer
398 ..Including texturizing storage node layer
399 ..Having contacts formed by selective growth or deposition
400 **FORMATION OF ELECTRICALLY ISOLATED LATERAL SEMICONDUCTIVE STRUCTURE**
401 .Having substrate registration feature (e.g., alignment mark)
402 .And gettering of substrate
403 .Having semi-insulating component
404 .Total dielectric isolation
405 ..And separate partially isolated semiconductor regions
406 ..Bonding of plural semiconductive substrates
407 ..Nondopant implantation
408 ..With electrolytic treatment step
409 ...Porous semiconductor formation
410 ..Encroachment of separate locally oxidized regions
411 ..Air isolation (e.g., beam lead supported semiconductor islands, etc.)
412 ...Semiconductor islands formed upon insulating substrate or layer (e.g., mesa isolation, etc.)
413 ..With epitaxial semiconductor formation
414 .Isolation by PN junction only
415 ..Thermomigration
416 ..With epitaxial semiconductor formation
417 ...And simultaneous polycrystalline growth
418 ...Dopant addition
419 ....Plural doping steps
420 ..Plural doping steps
421 .Having air-gap dielectric (e.g., groove, etc.)
422 ..Enclosed cavity
423 .Implanting to form insulator
424 .Grooved and refilled with deposited dielectric material
425 ..Combined with formation of recessed oxide by localized oxidation
426 ...Recessed oxide laterally extending from groove
427 ..Refilling multiple grooves of different widths or depths
428 ...Reflow of insulator
429 ..And epitaxial semiconductor formation in groove
430 ..And deposition of polysilicon or noninsulative material into groove
431 ...Oxidation of deposited material
432 ....Nonoxidized portions remaining in groove after oxidation
433 ..Dopant addition
434 ...From doped insulator in groove
435 ..Multiple insulative layers in groove
436 ...Reflow of insulator
437 ...Conformal insulator formation
438 ..Reflow of insulator
439 .Recessed oxide by localized oxidation (i.e., LOCOS)
440 ..Including nondopant implantation
441 ..With electrolytic treatment step
442 ..With epitaxial semiconductor layer formation
443 ..Etchback of recessed oxide
444 ..Preliminary etching of groove
445 ...Masking of groove sidewall
446 ....Polysilicon containing sidewall
447 ....Dopant addition
448 ..Utilizing oxidation mask having polysilicon component

449 ..Dopant addition
450 ...Implanting through recessed oxide
451 ...Plural doping steps
452 ..Plural oxidation steps to form recessed oxide
453 ..And electrical conductor formation (i.e., metallization)
454 .Field plate electrode
455 **BONDING OF PLURAL SEMICONDUCTOR SUBSTRATES**
456 .Having enclosed cavity
457 .Warping of semiconductor substrate
458 .Subsequent separation into plural bodies (e.g., delaminating, dicing, etc.)
459 .Thinning of semiconductor substrate
460 **SEMICONDUCTOR SUBSTRATE DICING**
461 .Beam lead formation
462 .Having specified scribe region structure (e.g., alignment mark, plural grooves, etc.)
463 .By electromagnetic irradiation (e.g., electron, laser, etc.)
464 .With attachment to temporary support or carrier
465 .Having a perfecting coating
466 **DIRECT APPLICATION OF ELECTRICAL CURRENT**
467 .To alter conductivity of fuse or antifuse element
468 .Electromigration
469 .Utilizing pulsed current
470 .Fusion of semiconductor region
471 **GETTERING OF SUBSTRATE**
472 .By vibrating or impacting
473 .By implanting or irradiating
474 ..Ionized radiation (e.g., corpuscular or plasma treatment, etc.)
475 ...Hydrogen plasma (i.e., hydrogenization)
476 .By layers which are coated, contacted, or diffused
477 .By vapor phase surface reaction
478 **FORMATION OF SEMICONDUCTIVE ACTIVE REGION ON ANY SUBSTRATE (E.G., FLUID GROWTH, DEPOSITION)**
479 .On insulating substrate or layer
480 ..Including implantation of ion which reacts with semiconductor substrate to form insulating layer
481 ..Utilizing epitaxial lateral overgrowth
482 .Amorphous semiconductor
483 ..Compound semiconductor
484 ..Running length (e.g., sheet, strip, etc.)
485 ..Deposition utilizing plasma (e.g., glow discharge, etc.)
486 ..And subsequent crystallization
487 ...Utilizing wave energy (e.g., laser, electron beam, etc.)
488 .Polycrystalline semiconductor
489 ..Simultaneous single crystal formation
490 ..Running length (e.g., sheet, strip, etc.)
491 ..And subsequent doping of polycrystalline semiconductor
492 .Fluid growth step with preceding and subsequent diverse operation
493 .Plural fluid growth steps with intervening diverse operation
494 ..Differential etching
495 ..Doping of semiconductor
496 ..Coating of semiconductive substrate with nonsemiconductive material
497 .Fluid growth from liquid combined with preceding diverse operation
498 ..Differential etching
499 ..Doping of semiconductor
500 .Fluid growth from liquid combined with subsequent diverse operation
501 ..Doping of semiconductor
502 ..Heat treatment
503 .Fluid growth from gaseous state combined with preceding diverse operation
504 ..Differential etching
505 ..Doping of semiconductor
506 ...Ion implantation
507 .Fluid growth from gaseous state combined with subsequent diverse operation
508 ..Doping of semiconductor
509 ..Heat treatment

510 **INTRODUCTION OF CONDUCTIVITY MODIFYING DOPANT INTO SEMICONDUCTIVE MATERIAL**
511 .Ordering or disordering
512 .Involving nuclear transmutation doping
513 .Plasma (e.g., glow discharge, etc.)
514 .Ion implantation of dopant into semiconductor region
515 ..Ionized molecules
516 ..Including charge neutralization
517 ..Of semiconductor layer on insulating substrate or layer
518 ..Of compound semiconductor
519 ...Including multiple implantation steps
520 ....Providing nondopant ion (e.g., proton, etc.)
521 ....Using same conductivity-type dopant
522 ...Including heat treatment
523 ...And contact formation (i.e., metallization)
524 ..Into grooved semiconductor substrate region
525 ..Using oblique beam
526 ..Forming buried region
527 ..Including multiple implantation steps
528 ...Providing nondopant ion (e.g., proton, etc.)
529 ...Using same conductivity-type dopant
530 ..Including heat treatment
531 ..Using shadow mask
532 ..Into polycrystalline region
533 ..And contact formation (i.e., metallization)
534 ...Rectifying contact (i.e., Schottky contact)
535 .By application of corpuscular or electromagnetic radiation (e.g., electron, laser, etc.)
536 ..Recoil implantation
537 .Fusing dopant with substrate (i.e., alloy junction)
538 ..Using additional material to improve wettability or flow characteristics (e.g., flux, etc.)
539 ..Application of pressure to material during fusion
540 ..Including plural controlled heating or cooling steps or nonuniform heating
541 ...Including diffusion after fusing step
542 .Diffusing a dopant
543 ..To control carrier lifetime (i.e., deep level dopant)
544 ..To solid-state solubility concentration
545 ..Forming partially overlapping regions
546 ..Plural dopants in same region (e.g., through same mask opening, etc.)
547 ...Simultaneously
548 ..Plural dopants simultaneously in plural regions
549 ..Single dopant forming plural diverse regions (e.g., forming regions of different concentrations or of different depths, etc.)
550 ..Nonuniform heating
551 ..Using multiple layered mask
552 ...Having plural predetermined openings in master mask
553 ..Using metal mask
554 ..Outwardly
555 ..Laterally under mask opening
556 ..Edge diffusion by using edge portion of structure other than masking layer to mask
557 ..From melt
558 ..From solid dopant source in contact with semiconductor region
559 ...Using capping layer over dopant source to prevent out-diffusion of dopant
560 ...Plural diffusion stages
561 ...Dopant source within trench or groove
562 ...Organic source
563 ...Glassy source or doped oxide
564 ...Polycrystalline semiconductor source
565 ..From vapor phase
566 ...Plural diffusion stages
567 ...Solid source in operative relation with semiconductor region
568 ....In capsule-type enclosure
569 ...Into compound semiconductor region

570 **FORMING SCHOTTKY JUNCTION (I.E., SEMICONDUCTOR-CONDUCTOR RECTIFYING JUNCTION CONTACT)**
571 .Combined with formation of ohmic contact to semiconductor region
572 .Compound semiconductor
573 ..Multilayer electrode
574 ...T-shaped electrode
575 ...Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)
576 ..Into grooved or recessed semiconductor region
577 ...Utilizing lift-off
578 ...Forming electrode of specified shape (e.g., slanted, etc.)
579 ....T-shaped electrode
580 .Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)
581 ..Silicide
582 .Using refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
583 ..Silicide
584 **COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL**
585 .Insulated gate formation
586 ..Combined with formation of ohmic contact to semiconductor region
587 ..Forming array of gate electrodes
588 ...Plural gate levels
589 ..Recessed into semiconductor substrate
590 ..Compound semiconductor
591 ..Gate insulator structure constructed of plural layers or nonsilicon containing compound
592 ..Possessing plural conductive layers (e.g., polycide)
593 ...Separated by insulator (i.e., floating gate)
594 ....Tunnelling dielectric layer
595 ..Having sidewall structure
596 ...Portion of sidewall structure is conductive
597 .To form ohmic contact to semiconductive material
598 ..Selectively interconnecting (e.g., customization, wafer scale integration, etc.)
599 ...With electrical circuit layout
600 ...Using structure alterable to conductive state (i.e., antifuse)
601 ...Using structure alterable to nonconductive state (i.e., fuse)
602 ..To compound semiconductor
603 ...II-VI compound semiconductor
604 ...III-V compound semiconductor
605 ....Multilayer electrode
606 ....Ga and As containing semiconductor
607 ..With epitaxial conductor formation
608 ..Oxidic conductor (e.g., indium tin oxide, etc.)
609 ...Transparent conductor
610 ..Conductive macromolecular conductor (including metal powder filled composition)
611 ..Beam lead formation
612 ..Forming solder contact or bonding pad
613 ...Bump electrode
614 ....Plural conductive layers
615 ....Including fusion of conductor
616 .....By transcription from auxiliary substrate
617 .....By wire bonding
618 ..Contacting multiple semiconductive regions (i.e., interconnects)
619 ...Air bridge structure
620 ...Forming contacts of differing depths into semiconductor substrate
621 ...Contacting diversely doped semiconductive regions (e.g., p-type and n-type regions, etc.)
622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
623 ....Including organic insulating material between metal levels

624 ....Separating insulating layer is laminate or composite of plural insulating materials
625 ....At least one metallization level formed of diverse conductive layers
626 .....Planarization
627 .....At least one layer forms a diffusion barrier
628 .....Having adhesion promoting layer
629 .....Diverse conductive layers limited to viahole/plug
630 ......Silicide formation
631 ....Having planarization step
632 .....Utilizing reflow
633 .....Simultaneously by chemical and mechanical means
634 .....Utilizing etch-stop layer
635 ....Insulator formed by reaction with conductor (e.g., oxidation, etc.)
636 ....Including use of antireflective layer
637 ....With formation of opening (i.e., viahole) in insulative layer
638 .....Having viaholes of diverse width
639 .....Having viahole with sidewall component
640 .....Having viahole of tapered shape
641 ....Selective deposition
642 ...Diverse conductors
643 ....At least one layer forms a diffusion barrier
644 ....Having adhesion promoting layer
645 ....Having planarization step
646 .....Utilizing reflow
647 ....Having electrically conductive polysilicon component
648 ....Having refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
649 .....Silicide
650 ....Having noble group metal (i.e., silver (Ag), gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)
651 .....Silicide
652 ..Plural layered electrode or conductor
653 ...At least one layer forms a diffusion barrier
654 ...Having adhesion promoting layer
655 ...Silicide
656 ...Having refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
657 ...Having electrically conductive polysilicon component
658 ..Altering composition of conductor
659 ...Implantation of ion into conductor
660 ..Including heat treatment of conductive layer
661 ...Subsequent fusing conductive layer
662 ....Utilizing laser
663 ...Rapid thermal anneal
664 ....Forming silicide
665 ..Utilizing textured surface
666 ..Specified configuration of electrode or contact
667 ...Conductive feedthrough or through-hole in substrate
668 ...Specified aspect ratio of conductor or viahole
669 ..And patterning of conductive layer
670 ...Utilizing lift-off
671 ...Utilizing multilayered mask
672 ...Plug formation (i.e., in viahole)
673 ...Tapered etching
674 ..Selective deposition of conductive layer
675 ...Plug formation (i.e., in viahole)
676 ...Utilizing electromagnetic or wave energy

677 ...Pretreatment of surface to enhance or retard deposition
678 ..Electroless deposition of conductive layer
679 ..Evaporative coating of conductive layer
680 ..Utilizing chemical vapor deposition (i.e., CVD)
681 ...Of organo-metallic precursor (i.e., MOCVD)
682 ..Silicide
683 ...Of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
684 ..Electrically conductive polysilicon
685 ..Refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
686 ..Noble group metal (i.e., silver (Ag), gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)
687 ..Copper of copper alloy conductor
688 ..Aluminum or aluminum alloy conductor
689 **CHEMICAL ETCHING**
690 .Combined with the removal of material by nonchemical means (e.g., ablating, abrading, etc.)
691 ..Combined mechanical and chemical material removal
692 ...Simultaneous (e.g., chemical-mechanical polishing, etc.)
693 ....Utilizing particulate abradant
694 .Combined with coating step
695 ..Simultaneous etching and coating
696 ..Coating of sidewall
697 ..Planarization by etching and coating
698 ...Utilizing reflow
699 ...Plural coating steps
700 ..Formation of groove or trench
701 ...Tapered configuration
702 ...Plural coating steps
703 ..Plural coating steps
704 .Having liquid and vapor etching steps
705 .Altering etchability of substrate region by compositional or crystalline modification
706 .Vapor phase etching (i.e., dry etching)
707 ..Utilizing electromagnetic or wave energy
708 ...Photo-induced etching
709 ....Photo-induced plasma etching
710 ...By creating electric field (e.g., plasma, glow discharge, etc.)
711 ....Utilizing multiple gas energizing means
712 ....Reactive ion beam etching (i.e., RIBE)
713 ....Forming tapered profile (e.g., tapered etching, etc.)
714 ....Including change in etch influencing parameter (e.g., energizing power, etchant composition, temperature, etc.)
715 ....With substrate heating or cooling
716 ....With substrate handling (e.g., conveying, etc.)
717 ....Utilizing multilayered mask
718 ....Compound semiconductor
719 ....Silicon
720 ....Electrically conductive material (e.g., metal, conductive oxide, etc.)
721 .....Silicide
722 ....Metal oxide
723 ....Silicon oxide or glass
724 ....Silicon nitride
725 ....Organic material (e.g., resist, etc.)
726 ....Having microwave gas energizing
727 .....Producing energized gas remotely located from substrate
728 ......Using magnet (e.g., electron cyclotron resonance, etc.)

729 ....Using specified electrode/susceptor configuration (e.g., of multiple substrates using barrel-type susceptor, planar reactor configuration, etc.) to generate plasma
730 .....Producing energized gas remotely located from substrate
731 ......Using intervening shield structure
732 ....Using magnet (e.g., electron cyclotron resonance, etc.)
733 ...Using or orientation dependent etchant (i.e., anisotropic etchant)
734 ..Sequential etching steps on a single layer
735 ..Differential etching of semiconductor substrate
736 ...Utilizing multilayered mask
737 ...Substrate possessing multiple layers
738 ....Selectively etching substrate possessing multiple layers of differing etch characteristics
739 .....Lateral etching of intermediate layer (i.e., undercutting)
740 .....Utilizing etch stop layer
741 ......PN junction functions as etch stop
742 ....Electrically conductive material (e.g., metal, conductive oxide, etc.)
743 ....Silicon oxide or glass
744 ....Silicon nitride
745 .Liquid phase etching
746 ..Utilizing electromagnetic or wave energy
747 ..With relative movement between substrate and confined pool of etchant
748 ..Projection of etchant against a moving substrate or controlling the angle or pattern of projected etchant
749 ..Sequential application of etchant
750 ...To same side of substrate
751 ....Each etch step exposes surface of an adjacent layer
752 ..Germanium
753 ..Silicon
754 ..Electrically conductive material (e.g., metal, conductive oxide, etc.)
755 ...Silicide
756 ..Silicon oxide
757 ..Silicon nitride
758 **COATING OF SUBSTRATE CONTAINING SEMICONDUCTOR REGION OR OF SEMICONDUCTOR SUBSTRATE**
759 .Combined with the removal of material by nonchemical means
760 .Utilizing reflow (e.g., planarization, etc.)
761 .Multiple layers
762 ..At least one layer formed by reaction with substrate
763 ..Layers formed of diverse composition or by diverse coating processes
764 .Formation of semi-insulative polycrystalline silicon
765 .By reaction with substrate
766 ..Implantation of ion (e.g., to form ion amorphousized region prior to selective oxidation, reacting with substrate to form insulative region, etc.)
767 ..Compound semiconductor substrate
768 ..Reaction with conductive region
769 ..Reaction with silicon semiconductive region (e.g., oxynitride formation, etc.)
770 ...Oxidation
771 ....Using electromagnetic or wave energy
772 .....Microwave gas energizing
773 ....In atmosphere containing water vapor (i.e., wet oxidation)
774 ....In atmosphere containing halogen
775 ...Nitridation
776 ....Using electromagnetic or wave energy
777 .....Microwave gas energizing
778 .Insulative material deposited upon semiconductive substrate
779 ..Compound semiconductor substrate
780 ..Depositing organic material (e.g., polymer, etc.)
781 ...Subsequent heating modifying organic coating composition

782 ..With substrate handling during coating (e.g., immersion, spinning, etc.)
783 ..Insulative material having impurity (e.g., for altering physical characteristics, etc.)
784 ...Introduction simultaneous with deposition
785 ..Insulative material is compound of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
786 ..Tertiary silicon containing compound formation (e.g., oxynitride formation, etc.)
787 ..Silicon oxide formation
788 ...Using electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)
789 ....Organic reactant
790 ...Organic reactant
791 ..Silicon nitride formation
792 ...Utilizing electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)
793 ....Organic reactant
794 ...Organic reactant
795 **RADIATION OR ENERGY TREATMENT MODIFYING PROPERTIES OF SEMICONDUCTOR REGION OF SUBSTRATE (E.G., THERMAL, CORPUSCULAR, ELECTROMAGNETIC, ETC.)**
796 .Compound semiconductor
797 ..Ordering or disordering
798 .Ionized irradiation (e.g., corpuscular or plasma treatment, etc.)
799 .By differential heating
800 **MISCELLANEOUS**

CROSS-REFERENCE ART COLLECTIONS

900 **BULK EFFECT DEVICE MAKING**
901 **CAPACITIVE JUNCTION**
902 **CAPPING LAYER**
903 **CATALYST AIDED DEPOSITION**
904 **CHARGE CARRIER LIFETIME CONTROL**
905 **CLEANING OF REACTION CHAMBER**
906 **CLEANING OF WAFER AS INTERIM STEP**
907 **CONTINUOUS PROCESSING**
908 .Utilizing cluster apparatus
909 **CONTROLLED ATMOSPHERE**
910 **CONTROLLING CHARGING STATE AT SEMICONDUCTOR-INSULATOR INTERFACE**
911 **DIFFERENTIAL OXIDATION AND ETCHING**
912 **DISPLACING PN JUNCTION**
913 **DIVERSE TREATMENTS PERFORMED IN UNITARY CHAMBER**
914 **DOPING**
915 .Amphoteric doping
916 .Autodoping control or utilization
917 .Deep level dopants (e.g., gold (Au), chromium (Cr), iron (Fe), nickel (Ni), etc.)
918 .Special or nonstandard dopant
919 .Compensation doping
920 .Controlling diffusion profile by oxidation
921 .Nonselective diffusion
922 .Diffusion along grain boundaries
923 .Diffusion through a layer
924 .To facilitate selective etching
925 .Fluid growth doping control (e.g., delta doping, etc.)
926 **DUMMY METALLIZATION**
927 **ELECTROMIGRATION RESISTANT METALLIZATION**
928 **FRONT AND REAR SURFACE PROCESSING**
929 **EUTECTIC SEMICONDUCTOR**
930 **TERNARY OR QUATERNARY SEMICONDUCTOR COMPRISED OF ELEMENTS FROM THREE DIFFERENT GROUPS (E.G., I-III-V, ETC.)**
931 **SILICON CARBIDE SEMICONDUCTOR**
932 **BORON NITRIDE SEMICONDUCTOR**
933 **GERMANIUM OR SILICON OR GE-SI ON III-V**
934 **SHEET RESISTANCE (I.E., DOPANT PARAMETERS)**
935 **GAS FLOW CONTROL**
936 **GRADED ENERGY GAP**
937 **HILLOCK PREVENTION**
938 **LATTICE STRAIN CONTROL OR UTILIZATION**
939 **LANGMUIR-BLODGETT FILM UTILIZATION**
940 **LASER ABLATIVE MATERIAL REMOVAL**
941 **LOADING EFFECT MITIGATION**

942 **MASKING**
943 .Movable
944 .Shadow
945 .Special (e.g., metal, etc.)
946 .Step and repeat
947 .Subphotolithographic processing
948 .Radiation resist
949 ..Energy beam treating radiation resist on semiconductor
950 ..Multilayer mask including nonradiation sensitive layer
951 ..Lift-off
952 ..Utilizing antireflective layer
953 **MAKING RADIATION RESISTANT DEVICE**
954 **MAKING OXIDE-NITRIDE-OXIDE DEVICE**
955 **MELT-BACK**
956 **MAKING MULTIPLE WAVELENGTH EMISSIVE DEVICE**
957 **MAKING METAL-INSULATOR-METAL DEVICE**
958 **PASSIVATION LAYER**
959 **MECHANICAL POLISHING OF WAFER**
960 **POROUS SEMICONDUCTOR**
961 **ION BEAM SOURCE AND GENERATION**
962 **QUANTUM DOTS AND LINES**
963 **REMOVING PROCESS RESIDUES FROM VERTICAL SUBSTRATE SURFACES**
964 **ROUGHENED SURFACE**
965 **SHAPED JUNCTION FORMATION**
966 **SELECTIVE OXIDATION OF ION-AMORPHOUSIZED LAYER**
967 **SEMICONDUCTOR ON SPECIFIED INSULATOR**
968 **SEMICONDUCTOR-METAL-SEMICONDUCTOR**
969 **SIMULTANEOUS FORMATION OF MONOCRYSTALLINE AND POLYCRYSTALLINE REGIONS**
970 **SPECIFIED ETCH STOP MATERIAL**
971 **STOICHIOMETRIC CONTROL OF HOST SUBSTRATE COMPOSITION**
972 **STORED CHARGE ERASURE**
973 **SUBSTRATE ORIENTATION**
974 **SUBSTRATE SURFACE PREPARATION**
975 **SUBSTRATE OR MASK ALIGNING FEATURE**
976 **TEMPORARY PROTECTIVE LAYER**
977 **THINNING OR REMOVAL OF SUBSTRATE**
978 **FORMING TAPERED EDGES ON SUBSTRATE OR ADJACENT LAYERS**
979 **TUNNEL DIODES**
980 **UTILIZING PROCESS EQUIVALENTS OR OPTIONS**
981 **UTILIZING VARYING DIELECTRIC THICKNESS**
982 **VARYING ORIENTATION OF DEVICES IN ARRAY**
983 **ZENER DIODES**

FOREIGN ART COLLECTIONS

FOR **CLASS-RELATED FOREIGN DOCUMENTS METHODS (156/1)**
FOR 100 .Etching of semiconductor precursor, substrates, and devices used in an electrical function (156/625.1)
FOR 101 ..Measuring, testing, or inspecting (156/626.1)
FOR 102 ...By electrical means or of electrical property (156/627.1)
FOR 103 ..Altering the etchability of a substrate by alloying, diffusing, or chemical reacting (156/628.1)
FOR 104 ..With uniting of preforms (e.g., laminating, etc.) (156/629.1)
FOR 105 ...Prior to etching (156/630.1)
FOR 106 ....Delamination subsequent to etching (156/631.1)
FOR 107 ....With coating (156/632.1)
FOR 108 ...Differential etching (156/633.1)
FOR 109 ....Metal layer etched (156/634.1)
FOR 110 ..With in situ activation or combining of etching components on surface (156/635.1)
FOR 111 ..With thin film of etchant between relatively moving substrate and conforming surface (e.g., chemical lapping, etc.) (156/636.1)
FOR 112 ..With relative movement between the substrate and a confined pool of etchant (156/637.1)
FOR 113 ...With removal of adhered reaction product from substrate (156/638.1)
FOR 114 ...With substrate rotation, repeated dipping, or advanced movement (156/639.1)

FOR 115 ..Projection of etchant against a moving substrate or controlling the angle or pattern of projected etchant (156/640.1)
FOR 116 ..Recycling or regenerating etchant (156/642.1)
FOR 117 ..With treatment by high energy radiation or plasma (e.g., ion beam, etc.) (156/643.1)
FOR 118 ..Forming or increasing the size of an aperture (156/644.1)
FOR 119 ..With mechanical deformation, severing, or abrading of a substrate (156/ 645.1)
FOR 120 ..Etchant is a gas (156/646.1)
FOR 121 ..Etching according to crystalline planes (156/647.1)
FOR 122 ..Etching isolates or modifies a junction in a barrier layer (156/648.1)
FOR 123 ...Discrete junction isolated (e.g., mesa formation, etc.) (156/649.1)
FOR 124 ..Sequential application of etchant material (156/650.1)
FOR 125 ...Sequentially etching the same surface of a substrate (156/651.1)
FOR 126 ....Each etching exposes surface of an adjacent layer (156/652.1)
FOR 127 .....Etched layer contains silicon (e.g., oxide, nitride, etc.) (156/653.1)
FOR 128 ..Differential etching of a substrate (156/654.1)
FOR 129 ...Composite substrate (156/655.1)
FOR 130 ....Substrate contains metallic element or compound (156/656.1)
FOR 131 ....Substrate contains silicon or silicon compound (156/657.1)
FOR 132 ...Resist coating (156/659.11)
FOR 133 ....Plural resist coating (156/661.11)
FOR 134 ..Silicon, germanium, or gallium containing substrate (156/662.1)
FOR 135 **MAKING DEVICE HAVING ORGANIC SEMICONDUCTOR COMPONENT (437/1)**
FOR 136 **MAKING DEVICE RESPONSIVE TO RADIATION (437/2)**
FOR 137 .Radiation detectors, e.g., infrared, etc. (437/3)
FOR 138 .Composed of polycrystalline material (437/4)
FOR 139 .Having semiconductor compound (437/5)
FOR 140 **MAKING THYRISTOR, E.G., DIAC, TRIAC, ETC. (437/6)**
FOR 141 **INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION (437/7)**
FOR 142 **INCLUDING TESTING OR MEASURING (437/8)**
FOR 143 **INCLUDING APPLICATION OF VIBRATORY FORCE (437/9)**
FOR 144 **INCLUDING GETTERING (437/10)**
FOR 145 .By ion implanting or irradiating (437/11)
FOR 146 .By layers which are coated, contacted, or diffused (437/12)
FOR 147 .By vapor phase surface reaction (437/13)
FOR 148 **THERMOMIGRATION (437/14)**
FOR 149 **INCLUDING FORMING A SEMICONDUCTOR JUNCTION (437/15)**
FOR 150 .Using energy beam to introduce dopant or modify dopant distribution (437/ 16)
FOR 151 ..Neutron, gamma ray or electron beam (437/17)
FOR 152 ..Ionized molecules (437/18)
FOR 153 ..Coherent light beam (437/19)
FOR 154 ..Ion beam implantation (437/20)
FOR 155 ..Of semiconductor on insulating substrate (437/21)
FOR 156 ...Of semiconductor compound (437/22)
FOR 157 ....Light emitting diode (LED) (437/23)
FOR 158 ...Providing nondopant ion including proton (437/24)
FOR 159 ...Providing auxiliary heating (437/25)
FOR 160 ...Forming buried region (437/26)
FOR 161 ...Including multiple implantations of same region (437/27)
FOR 162 ....Through insulating layer (437/28)
FOR 163 .....Forming field effect transistor (FET) type device (437/29)
FOR 164 ....Using same conductivity type dopant (437/30)

FOR 165 ....Forming bipolar transistor (NPN/PNP) (437/31)
FOR 166 .....Lateral bipolar transistor (437/32)
FOR 167 .....Having dielectric isolation (437/33)
FOR 168 ....Forming complementary MOS (metal oxide semiconductor) (437/34)
FOR 169 ...Using oblique beam (437/35)
FOR 170 ...Using shadow mask (437/36)
FOR 171 ...Having projected range less than thickness of dielectrics on substrate (437/37)
FOR 172 ...Into shaped or grooved semiconductor substrate (437/38)
FOR 173 ...Involving Schottky contact formation (437/39)
FOR 202 ....Gate structure constructed of diverse dielectrics (437/42)
FOR 203 .....Gate surrounded by dielectric layer, e.g., floating gate, etc. (437/43)
FOR 204 .....Adjusting channel dimension (437/44)
FOR 205 .....Active step for controlling threshold voltage (437/45)
FOR 185 .....Self-aligned (437/41 R)
FOR 186 .....With bipolar (437/41 RBP)
FOR 187 .....CMOS (437/41 RCM)
FOR 188 .....Lightly doped drain (437/41 RLD)
FOR 189 .....Memory devices (437/41 RMM)
FOR 190 .....Asymmetrical FET (437/41 AS)
FOR 191 .....Channel specifics (437/41 CS)
FOR 192 .....DMOS/vertical FET (437/41 DM)
FOR 193 .....Gate specifics (437/41 GS)
FOR 194 .....Junction FET/static induction transistor (437/41 JF)
FOR 195 .....Layered channel (437/41 LC)
FOR 196 .....Specifics of metallization/ contact (437/41 SM)
FOR 197 .....Recessed gate (Schottky falls below in SH) (437/41 RG)
FOR 198 .....Schottky gate/MESFET (437/41 SH)
FOR 199 .....Sidewall (437/41 SW)
FOR 200 .....Thin film transistor, inverted (437/41 TFI)
FOR 201 .....Thin film transistor (437/41 TFT)
FOR 174 ....Forming pair of device regions separated by gate structure, i.e., FET (437/40 R)
FOR 175 ....Asymmetrical FET (any asymmetry in S/D profile, gate spacing, etc.) (437/40 AS)
FOR 176 ....DMOS/vertical FET (437/40 DM)
FOR 177 ....Gate specific (specifics of gate insulator/structure/ material/ contact) (437/40 GS)
FOR 178 ....Junction FET/static induction transistor (437/40 JF)
FOR 179 ....Layered channel (e.g., HEMT, MODFET, 2DEG, heterostructure FETS) (437/40 LC)
FOR 180 ....Recessed gate (437/40 RG)
FOR 181 ....Schottky gate/MESFET (controls over RG) (437/40 SH)
FOR 182 ....Sidewall (not LDD's) (437/40 SW)
FOR 183 ....Thin film transistor inverted/staggered (437/40 TFI)
FOR 184 ....Thin film transistor (437/40 TFT)
FOR 206 ...Into polycrystalline or polyamorphous regions (437/46)
FOR 207 ...Integrating active with passive devices (437/47)
FOR 208 ...Forming plural active devices in grid/array, e.g., RAMS/ ROMS, etc. (437/48)
FOR 209 ....Having multiple-level electrodes (437/49)
FOR 210 ...Forming electrodes in laterally spaced relationships (437/50)
FOR 211 .Making assemblies of plural individual devices having community feature, e.g., integrated circuit, electrical connection, etc. (437/51)
FOR 212 ..Memory devices (437/52)
FOR 213 ..Charge coupled devices (CCD) (437/53)
FOR 214 ..Diverse types (437/54)
FOR 215 ...Integrated injection logic (I2L) circuits (437/55)
FOR 216 ...Plural field effect transistors (CMOS) (437/56)
FOR 217 ....Complementary metal oxide having diverse conductivity source and drain regions (437/57)

FOR 218 ....Having like conductivity source and drain regions (437/58)
FOR 219 ...Including field effect transistor (437/59)
FOR 220 ...Including passive device (437/60)
FOR 221 .Including isolation step (437/61)
FOR 222 ..By forming total dielectric isolation (437/62)
FOR 223 ..By forming vertical isolation combining dielectric and PN junction (437/63)
FOR 224 ..Using vertical dielectric (air-gap/insulator) and horizontal PN junction (437/64)
FOR 225 ...Grooved air-gap only (437/65)
FOR 226 ....V-groove (437/66)
FOR 227 ...Grooved and refilled with insulator (437/67)
FOR 228 ....V-groove (437/68)
FOR 229 ...Recessed oxide by localized oxidation (437/69)
FOR 230 ....Preliminary formation of guard ring (437/70)
FOR 231 ....Preliminary anodizing (437/71)
FOR 232 ....Preliminary etching of groove (437/72)
FOR 233 .....Using overhanging oxidation mask and pretreatment of recessed walls (437/ 73)
FOR 234 ..Isolation by PN junction only (437/74)
FOR 235 ...By diffusion from upper surface only (437/75)
FOR 236 ...By up-diffusion from substrate region and down diffusion into upper surface layer (437/76)
FOR 237 ....Substrate and epitaxial regions of same conductivity type, i.e., P or N (437/77)
FOR 238 ...By etching and refilling with semiconductor material having diverse conductivity (437/78)
FOR 239 ...Using polycrystalline region (437/79)
FOR 240 .Shadow masking (437/80)
FOR 241 .Doping during fluid growth of semiconductor material on substrate (437/81)
FOR 242 ..Including heat to anneal (437/82)
FOR 243 ..Growing single crystal on amorphous substrate (437/83)
FOR 244 ..Growing single crystal on single crystal insulator (SOS) (437/84)
FOR 245 ..Including purifying stage during growth (437/85)
FOR 246 ..Using transitory substrate (437/86)
FOR 247 ..Using inert atmosphere (437/87)
FOR 248 ..Using catalyst to alter growth process (437/88)
FOR 249 ..Growth through opening (437/89)
FOR 250 ...Forming recess in substrate and refilling (437/90)
FOR 251 ....By liquid phase epitaxy (437/91)
FOR 252 ...By liquid phase epitaxy (437/92)
FOR 253 ..Specified crystal orientation other than (100) or (111) planes (437/93)
FOR 254 ..Introducing minority carrier life time reducing dopant during growth, i.e., deep level dopant Au (Gold), Cr (Cromium), Fe (Iron), Ni (Nickel), etc. (437/94)
FOR 255 ..Autodoping control (437/95)
FOR 256 ...Compound formed from Group III and Group V elements (437/96)
FOR 257 ..Forming buried regions with outdiffusion control (437/97)
FOR 258 ...Plural dopants simultaneously outdiffusioned (437/98)
FOR 259 ..Growing mono and polycrystalline regions simultaneously (437/99)
FOR 260 ..Growing silicon carbide (SiC) (437/100)
FOR 261 ..Growing amorphous semiconductor material (437/101)
FOR 262 ..Source and substrate in close-space relationship (437/102)
FOR 263 ...Group IV elements (437/103)
FOR 264 ...Compound formed from Group III and Group V elements (437/104)
FOR 265 ..Vacuum growing using molecular beam, i.e., vacuum deposition (437/105)
FOR 266 ...Group IV elements (437/106)
FOR 267 ...Compound formed from Group III and Group V elements (437/107)
FOR 268 ..Growing single layer in multi-steps (437/108)

FOR 269 ...Polycrystalline layers (437/109)
FOR 270 ...Using modulated dopants or materials, e.g., superlattice, etc. (437/110)
FOR 271 ...Using preliminary or intermediate metal layer (437/111)
FOR 272 ...Growing by varying rates (437/112)
FOR 273 ..Using electric current, e.g., Peltier effect, glow discharge, etc. (437/ 113)
FOR 274 ..Using seed in liquid phase (437/114)
FOR 275 ...Pulling from melt (437/115)
FOR 276 ....And diffusing (437/116)
FOR 277 ..Liquid and vapor phase epitaxy in sequence (437/117)
FOR 278 ..Involving capillary action (437/118)
FOR 279 ..Sliding liquid phase epitaxy (437/119)
FOR 280 ...Modifying melt composition (437/120)
FOR 281 ...Controlling volume or thickness of growth (437/121)
FOR 282 ...Preliminary dissolving substrate surface (437/122)
FOR 283 ...With nonlinear slide movement (437/123)
FOR 284 ...One melt simultaneously contacting plural substrates (437/124)
FOR 285 ..Tipping liquid phase epitaxy (437/125)
FOR 286 ..Heteroepitaxy (437/126)
FOR 287 ...Multi-color light emitting diode (LED) (437/127)
FOR 288 ...Graded composition (437/128)
FOR 289 ...Forming laser (437/129)
FOR 290 ...By liquid phase epitaxy (437/130)
FOR 291 ...Si (Silicon on Ge (Germanium) or Ge (Germanium) on Si (Silicon) (437/131)
FOR 292 ...Either Si (Silicon) or Ge (Germanium) layered with or on compound formed from Group III and Group V elements (437/132)
FOR 293 ...Compound formed from Group III and Group V elements on diverse Group III and Group V including substituted Group III and Group V compounds (437/133)
FOR 294 .By fusing dopant with substrate, e.g., alloying, etc. (437/134)
FOR 295 ..Using flux (437/135)
FOR 296 ..Passing electric current through material (437/136)
FOR 297 ..With application of pressure to material during fusing (437/137)
FOR 298 ..Including plural controlled heating or cooling steps (437/138)
FOR 299 ..Including diffusion after fusion step (437/139)
FOR 300 ..Including additional material to improve wettability or flow characteristics (437/140)
FOR 301 .Diffusing a dopant (437/141)
FOR 302 ..To control carrier lifetime, i.e., deep level dopant Au (Gold), Cr (Chromium), Fe (Iron), Ni (Nickel), etc. (437/142)
FOR 303 ..Al (Aluminum) dopant (437/143)
FOR 304 ..Li (Lithium) dopant (437/144)
FOR 305 ..Including nonuniform heating (437/145)
FOR 306 ..To solid state solubility concentration (437/146)
FOR 307 ..Using multiple layered mask (437/147)
FOR 308 ...Having plural predetermined openings in master mask (437/148)
FOR 309 ..Forming partially overlapping regions (437/149)
FOR 310 ..Plural dopants in same region, e.g., through same mask opening, etc. (437/150)
FOR 311 ...Simultaneously (437/151)
FOR 312 ..Plural dopants simultaneously in plural region (437/152)
FOR 313 ..Single dopant forming plural diverse regions (437/153)
FOR 314 ...Forming regions of different concentrations or different depths (437/154)
FOR 315 ..Using metal mask (437/155)
FOR 316 ..Outwardly (437/156)
FOR 317 ..Laterally under mask (437/157)

FOR 318 ..Edge diffusion by using edge portion of structure other than masking layer to mask (437/158)
FOR 319 ..From melt (437/159)
FOR 320 ..From solid dopant source in contact with substrate (437/160)
FOR 321 ...Using capping layer over dopant source to prevent outdiffusion of dopant (437/161)
FOR 322 ...Polycrystalline semiconductor source (437/162)
FOR 323 ...Organic source (437/163)
FOR 324 ...Glassy source or doped oxide (437/164)
FOR 325 ..From vapor phase (437/165)
FOR 326 ...In plural stages (437/166)
FOR 327 ...Zn (Zinc) dopant (437/167)
FOR 328 ...Solid source is operative relation with semiconductor material (437/168)
FOR 329 ....In capsule type enclosure (437/169)
FOR 330 **DIRECTLY APPLYING ELECTRICAL CURRENT (437/170)**
FOR 331 .And regulating temperature (437/171)
FOR 332 .Alternating or pulsed current (437/172)
FOR 333 **APPLYING CORPUSCULAR OR ELECTROMAGNETIC ENERGY (437/173)**
FOR 334 .To anneal (437/174)
FOR 335 **FORMING SCHOTTKY CONTACT (437/175)**
FOR 336 .On semiconductor compound (437/176)
FOR 337 ..Multi-layer electrode (437/177)
FOR 338 .Using platinum group silicide, i.e., silicide of Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium) (437/178)
FOR 339 .Using metal, i.e., Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium), Au (Gold), Ag (Silver) (437/179)
FOR 340 **MAKING OR ATTACHING ELECTRODE ON OR TO SEMICONDUCTOR, OR SECURING COMPLETED SEMICONDUCTOR TO MOUNTING OR HOUSING (437/180)**
FOR 341 .Forming transparent electrode (437/181)
FOR 342 .Forming beam electrode (437/182)
FOR 343 .Forming bump electrode (437/183)
FOR 344 .Electrode formed on substrate composed of elements of Group III and Group V semiconductor compound (437/184)
FOR 345 .Electrode formed on substrate composed of elements of Group II and Group VI semiconductor compound (437/185)
FOR 346 .Single polycrystalline electrode layer on substrate (437/186)
FOR 347 .Single metal layer electrode on substrate (437/187)
FOR 348 ..Subsequently fusing, e.g., alloying, sintering, etc. (437/188)
FOR 349 .Forming plural layered electrode (437/189)
FOR 350 ..Including central layer acting as barrier between outer layers (437/190)
FOR 351 ..Of polysilicon only (437/191)
FOR 352 ..Including refractory metal layer of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten) (437/192)
FOR 353 ..Including polycrystalline silicon layer (437/193)
FOR 354 ..Including Al (Aluminum) layer (437/194)
FOR 355 ..Including layer separated by insulator (437/195)
FOR 356 .Forming electrode of alloy or electrode of a compound of Si (Silicon) (437/196)
FOR 357 ..Al (Aluminum) alloy (437/197)
FOR 358 ...Including Cu (Copper) (437/198)
FOR 359 ...Including Si (Silicon) (437/199)

FOR 360 ..Silicide of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten), (437/200)
FOR 361 ..Of plantinum metal group Ru (Ruthenium), Rh (Rhodium), Pd (Palladium), Os (Osmium), Ir (Iridium), Pt (Platinum) (437/201)
FOR 362 ..By fusing metal with semiconductor (alloying) (437/202)
FOR 363 .Depositing electrode in preformed recess in substrate (437/203)
FOR 364 .Including positioning of point contact (437/204)
FOR 365 .Making plural devices (437/205)
FOR 366 ..Using strip lead frame (437/206)
FOR 367 ...And encapsulating (437/207)
FOR 368 ..Stacked array, e.g., rectifier, etc. (437/208)
FOR 369 .Securing completed semiconductor to mounting, housing or external lead (437/209)
FOR 370 ..Including contaminant removal (437/210)
FOR 371 ..Utilizing potting or encapsulating material only to surround leads and device to maintain position, i.e. without housing (437/211)
FOR 372 ...Including application of pressure (437/212)
FOR 373 ...Glass material (437/213)
FOR 374 ..Utilizing header (molding surface means) (437/214)
FOR 375 ..Insulating housing (437/215)
FOR 376 ...Including application of pressure (437/216)
FOR 377 ...And lead frame (437/217)
FOR 378 ...Ceramic housing (437/218)
FOR 379 ...Including encapsulating (437/219)
FOR 380 ..Lead frame (437/220)
FOR 381 ..Metallic housing (437/221)
FOR 382 ...Including application of pressure (437/222)
FOR 383 ...Including glass support base (437/223)
FOR 384 ...Including encapsulating (437/224)
FOR 385 **INCLUDING COATING OR MATERIAL REMOVAL, E.G., ETCHING, GRINDING, ETC. (437/ 225)**
FOR 386 .Substrate dicing (437/226)
FOR 387 ..With a perfecting coating (437/227)
FOR 388 .Coating and etching (437/228)
FOR 389 .Of radiation resist layer (437/229)
FOR 390 .By immersion metal plating from solution, i.e., electroless plating (437/230)
FOR 391 .By spinning (437/231)
FOR 392 .Elemental Se (Selenium) substrate or coating (437/232)
FOR 393 .Of polycrystalline semiconductor material on substrate (437/233)
FOR 394 ..Semiconductor compound or mixed semiconductor material (437/234)
FOR 395 .Of a dielectric or insulative material (437/235)
FOR 396 ..Containing Group III atom (437/236)
FOR 397 ...By reacting with substrate (437/237)
FOR 398 ..Monoxide or dioxide or Ge (Germanium) or Si (Silicon) (437/238)
FOR 399 ...By reacting with substrate (437/239)
FOR 400 ...Doped with impurities (437/240)
FOR 401 ..Si (Silicon) and N (Nitrogen) (437/241)
FOR 402 ...By chemical reaction with substrate (437/242)
FOR 403 ..Directly on semiconductor substrate (437/243)
FOR 404 ...By chemical conversion of substrate (437/244)
FOR 405 .Comprising metal layer (437/245)
FOR 406 ..On metal (437/246)
FOR 407 **TEMPERATURE TREATMENT MODIFYING PROPERTIES OF SEMICONDUCTOR, E.G., ANNEALING, SINTERING, ETC. (437/247)**
FOR 408 .Heating and cooling (437/248)
FOR 409 **INCLUDING SHAPING (437/249)**
FOR 410 **MISCELLANEOUS (437/250)**
FOR 411 **UTILIZING PROCESS EQUIVALENTS OR OPTIONS (437/900)**
FOR 412 **MAKING PRESSURE SENSITIVE DEVICE (437/901)**

FOR 413 **MAKING DEVICE HAVING HEAT SINK (437/902)**
FOR 414 **MAKING THERMOPILE (437/903)**
FOR 415 **MAKING DIODE (437/904)**
FOR 416 .Light emmitting diode (437/905)
FOR 417 ..Mounting and contact (437/906)
FOR 418 **LASER PROCESSING OF FIELD EFFECT TRANSISTOR (FET) (437/907)**
FOR 419 **LASER PROCESSING OF TRANSISTOR (437/908)**
FOR 420 **MAKING TRANSISTOR ONLY (437/909)**
FOR 421 **MAKING JOSEPHSON JUNCTION DEVICE (437/910)**
FOR 422 **MAKING JUNCTION-FIELD EFFECT TRANSISTOR (J-FET) OR STATIC INDUCTION THYRSISTOR (SIT) DEVICE (437/911)**
FOR 423 **MAKING METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MESFET) DEVICE ONLY (437/912)**
FOR 424 **MAKING METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET) DEVICE (437/913)**
FOR 425 **MAKING NON-EPITAXIAL DEVICE (437/914)**
FOR 426 **MAKING VERTICALLY STACKED DEVICES (3-DIMENSIONAL STRUCTURE) (437/915)**
FOR 427 **MAKING PHOTOCATHODE OR VIDICON (437/916)**
FOR 428 **MAKING LATERAL TRANSISTOR (437/917)**
FOR 429 **MAKING RESISTOR (437/918)**
FOR 430 **MAKING CAPACITOR (437/919)**
FOR 431 **MAKING SILICON-OXIDE-NITRIDE-OXIDE ON SILICON (SONOS) DEVICE (437/920)**
FOR 432 **MAKING STRAIN GAGE (437/921)**
FOR 433 **MAKING FUSE OR FUSABLE DEVICE (437/922)**
FOR 434 **WITH REPAIR OR RECOVERY OF DEVICE (437/923)**
FOR 435 **HAVING SUBSTRATE OR MASK ALIGNING FEATURE (437/924)**
FOR 436 **SUBSTRATE SUPPORT OR CAPSULE CONSTRUCTION (437/925)**
FOR 437 **CONTINUOUS PROCESSING (437/926)**
FOR 438 **FORMING HOLLOW BODIES AND ENCLOSED CAVITIES (437/927)**
FOR 439 **ENERGY BEAM TREATING RADIATION RESIST ON SEMICONDUCTOR (437/928)**
FOR 440 **RADIATION ENHANCED DIFFUSION (R.E.D.) (437/929)**
FOR 441 **ION BEAM SOURCE AND GENERATION (437/930)**
FOR 442 **IMPLANTATION THROUGH MASK (437/931)**
FOR 443 **RECOIL IMPLANTATION (437/932)**
FOR 444 **DUAL SPECIES IMPLANTATION OF SEMICONDUCTOR (437/933)**
FOR 445 **DOPANT ACTIVATION PROCESS (437/934)**
FOR 446 **BEAM WRITING OF PATTERNS (437/935)**
FOR 447 **BEAM PROCESSING OF COMPOUND SEMICONDUCTOR DEVICE (437/936)**
FOR 448 **HYDROGEN PLASMA TREATMENT OF SEMICONDUCTOR DEVICE (437/937)**
FOR 449 **MAKING RADIATION RESISTANT DEVICE (437/938)**
FOR 450 **DEFECT CONTROL OF SEMICONDUCTOR WAFER (PRETREATMENT) (437/939)**
FOR 451 **SELECTIVE OXIDATION OF ION AMORPHOUSIZED LAYERS (437/940)**
FOR 452 **CONTROLLING CHARGING STATE AT SEMICONDUCTOR-INSULATOR INTERFACE (437/941)**
FOR 453 **INCOHERENT LIGHT PROCESSING (437/942)**
FOR 454 **THERMALLY ASSISTED BEAM PROCESSING (437/943)**
FOR 455 **UTILIZING LIFT OFF (437/944)**
FOR 456 **STOICHIOMETRIC CONTROL OF HOST SUBSTRATE COMPOSITION (437/945)**
FOR 457 **SUBSTRATE SURFACE PREPARATION (437/946)**
FOR 458 **FORMING TAPERED EDGES ON SUBSTRATE OR ADJACENT LAYERS (437/947)**
FOR 459 **MOVABLE MASK (437/948)**
FOR 460 **CONTROLLED ATMOSPHERE (437/949)**
FOR 461 **SHALLOW DIFFUSION (437/950)**
FOR 462 **AMPHOTERIC DOPING (437/951)**
FOR 463 **CONTROLLING DIFFUSION PROFILE BY OXIDATION (437/952)**
FOR 464 **DIFFUSION OF OVERLAPPING REGIONS (COMPENSATION) (437/953)**
FOR 465 **VERTICAL DIFFUSION THROUGH A LAYER (437/954)**
FOR 466 **NONSELECTIVE DIFFUSION (437/955)**
FOR 467 **DISPLACING P-N JUNCTION (437/956)**
FOR 468 **ELECTROMIGRATION (437/957)**
FOR 469 **SHAPED JUNCTION FORMATION (437/958)**
FOR 470 **USING NONSTANDARD DOPANT (437/959)**
FOR 471 **WASHED EMITTER PROCESS (437/960)**

FOR 472 **EMITTER DIP PREVENTION (OR UTILIZATION) (437/961)**
FOR 473 **UTILIZING SPECIAL MASKS (CARBON, ETC.) (437/962)**
FOR 474 **LOCALIZED HEATING CONTROL DURING FLUID GROWTH (437/963)**
FOR 475 **FLUID GROWTH INVOLVING VAPOR-LIQUID-SOLID STAGES (437/964)**
FOR 476 **FLUID GROWTH OF COMPOUNDS COMPOSED OF GROUPS II, IV, OR VI ELEMENTS (437/965)**
FOR 477 **FORMING THIN SHEETS (437/966)**
FOR 478 **PRODUCING POLYCRYSTALLINE SEMICONDUCTOR MATERIAL (437/967)**
FOR 479 **SELECTIVE OXIDATION OF POLYCRYSTALLINE LAYER (437/968)**
FOR 480 **FORMING GRADED ENERGY GAP LAYERS (437/969)**
FOR 481 **DIFFERENTIAL CRYSTAL GROWTH (437/970)**
FOR 482 **FLUID GROWTH DOPING CONTROL (437/971)**
FOR 483 **UTILIZING MELT-BACK (437/972)**
FOR 484 **SOLID PHASE EPITAXIAL GROWTH (437/973)**
FOR 485 **THINNING OR REMOVAL OF SUBSTRATE (437/974)**
FOR 486 **DIFFUSION ALONG GRAIN BOUNDARIES (437/975)**
FOR 487 **CONTROLLING LATTICE STRAIN (437/976)**
FOR 488 **UTILIZING ROUGHENED SURFACE (437/977)**
FOR 489 **UTILIZING MULTIPLE DIELECTRIC LAYERS (437/978)**
FOR 490 **UTILIZING THICK-THIN OXIDE FORMATION (437/979)**
FOR 491 **FORMING POLYCRYSTALLINE SEMICONDUCTOR PASSIVATION (437/980)**
FOR 492 **PRODUCING TAPERED ETCHING (437/981)**
FOR 493 **REFLOW OF INSULATOR (437/982)**
FOR 494 **OXIDATION OF GATE OR GATE CONTACT LAYER (437/983)**
FOR 495 **SELF-ALIGNING FEATURE (437/984)**
FOR 496 **DIFFERENTIAL OXIDATION AND ETCHING (437/985)**
FOR 497 **DIFFUSING LATERALLY AND ETCHING (437/986)**
FOR 498 **DIFFUSING DOPANTS IN COMPOUND SEMICONDUCTOR (437/987)**